



SSC8L84PN6

N-Channel Enhancement Mode MOSFET

➤ Features

V_{DS}	V_{GS}	$R_{DS(ON)}$ Typ.	I_D
80V	$\pm 20V$	2.1m Ω @10V	130A
		2.7m Ω @6V0	

➤ Description

This device is N-Channel enhancement MOSFET. Uses SGT technology and design to provide excellent RDSON with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit.

100% UIS + ΔV_{DS} + R_g Tested!

➤ Applications

- Load Switch
- PWM Application
- Power Management
- DC-DC Conversion

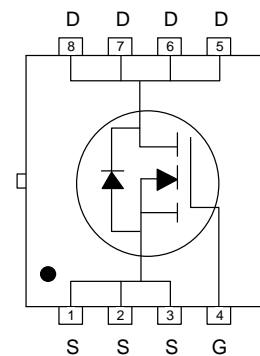
➤ Ordering Information

Device	Package	Shipping
SSC8L84PN6	PDFN5X6-8L	5000/Reel

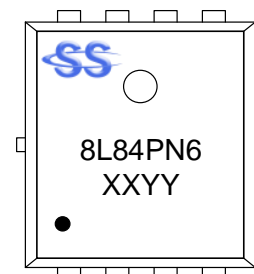
➤ Pin configuration



PDFN5X6-8L



Pin Configuration (Top View)



Marking

(XYYY: Internal Traceability Code)

**➤ Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)**

Symbol	Parameter		Ratings	Unit
V_{DS}	Drain-to-Source Voltage		80	V
V_{GS}	Gate-to-Source Voltage		± 20	V
I_D	Continuous Drain Current ^d	$T_C=25^{\circ}\text{C}$	130	A
		$T_C=100^{\circ}\text{C}$	80	
I_{DSM}	Continuous Drain Current ^a	$T_A=25^{\circ}\text{C}$	24	A
		$T_A=70^{\circ}\text{C}$	16	
I_{DM}	Pulsed Drain Current ^b		580	A
P_D	Power Dissipation ^c	$T_C=25^{\circ}\text{C}$	83.3	W
		$T_C=100^{\circ}\text{C}$	33.3	
P_{DSM}	Power Dissipation ^a	$T_A=25^{\circ}\text{C}$	2.1	W
		$T_A=70^{\circ}\text{C}$	1.3	
I_{AS}	Avalanche Current ^b $L=0.5\text{mH}$ Single Pulse		48	A
E_{AS}	Avalanche Energy ^b $L=0.5\text{mH}$ Single Pulse		576	mJ
T_J	Operation junction temperature		-55~150	$^{\circ}\text{C}$
T_{STG}	Storage temperature range		-55~150	

➤ Thermal Resistance Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Max.	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ^a	60	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	1.5	

Note:

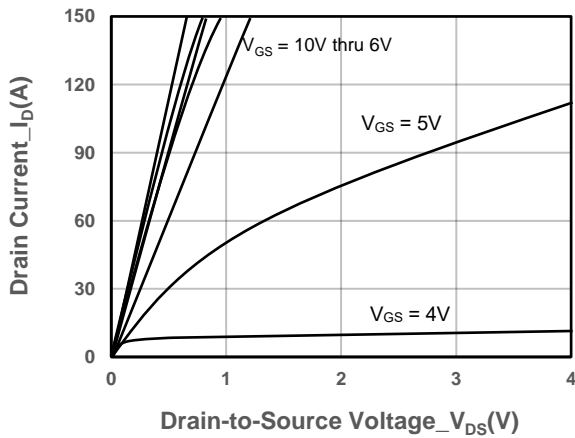
- The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The value in any given application depends on the user is specific board design. The power dissipation is based on the $t \leq 10\text{s}$ thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation P_D is based on $T_{J(MAX)}=150^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.
- The maximum current rating is package limited.

➤ **Electrical Characteristics (T_A=25°C unless otherwise noted)**

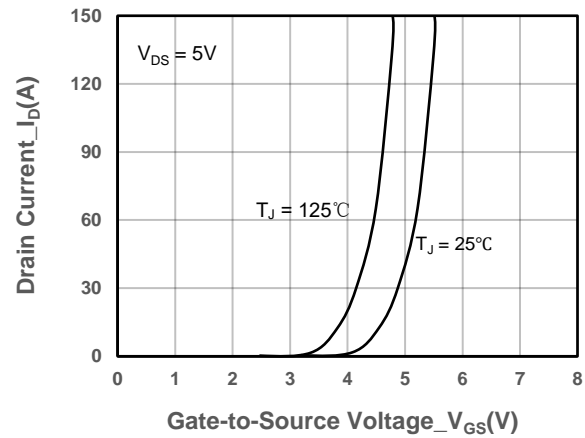
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	80			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250uA	2	2.8	4	V
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D = 20A		2.1	2.7	mΩ
		V _{GS} = 6V, I _D = 10A		2.7	3.5	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80V, V _{GS} = 0V			1	μA
Gate-Source Leak Current	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V			±100	nA
Forward Voltage	V _{SD}	V _{GS} = 0V, I _S = 10A		0.8	1.4	V
Gate Resistance	R _G	V _{DS} = 0V, f = 1MHz		2.2		Ω
Input Capacitance	C _{ISS}	V _{DS} = 40V, V _{GS} = 0V, f = 1MHz		4950		pF
Output Capacitance	C _{OSS}			1590		
Reverse Transfer Capacitance	C _{RSS}			30		
Total Gate Charge	Q _G	V _{GS} = 10V, V _{DS} = 40V, I _D = 20A		45		nC
Gate to Source Charge	Q _{GS}			15		
Gate to Drain Charge	Q _{GD}			12		
Turn-on Delay Time	T _{D(ON)}	V _{GS} = 10V, V _{DS} = 40V, R _L = 2Ω, R _G = 3Ω,		20		ns
Rise Time	T _r			28		
Turn-off Delay Time	T _{D(OFF)}			30		
Fall Time	T _f			9		
Diode Recovery Time	T _{rr}	I _F =20A, di/dt=100A/us		60		ns
Diode Recovery Charge	Q _{rr}	I _F =20A, di/dt=100A/us		85		nC



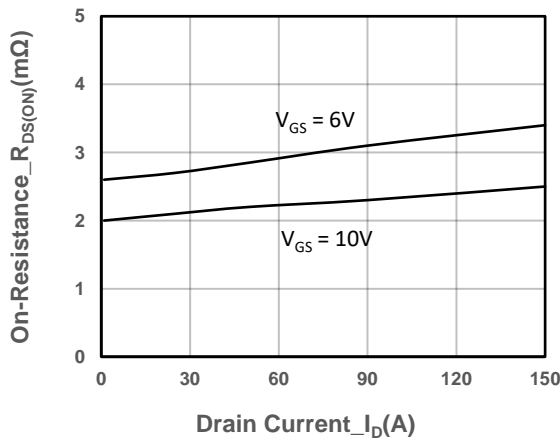
➤ Typical Performance Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)



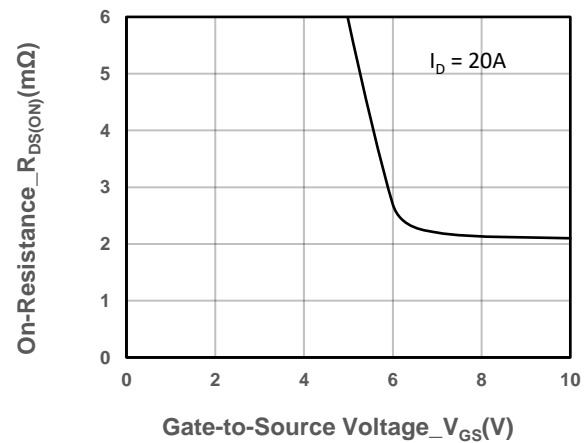
Output Characteristics



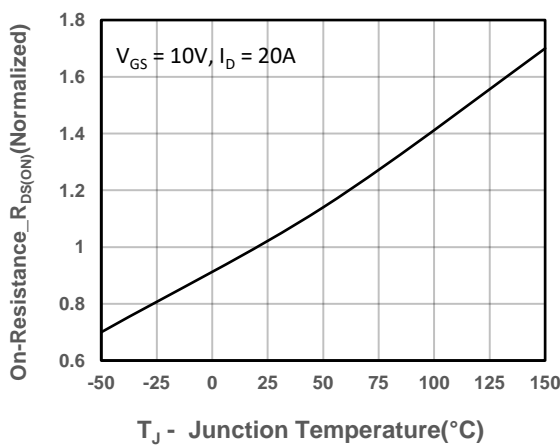
Transfer Characteristics



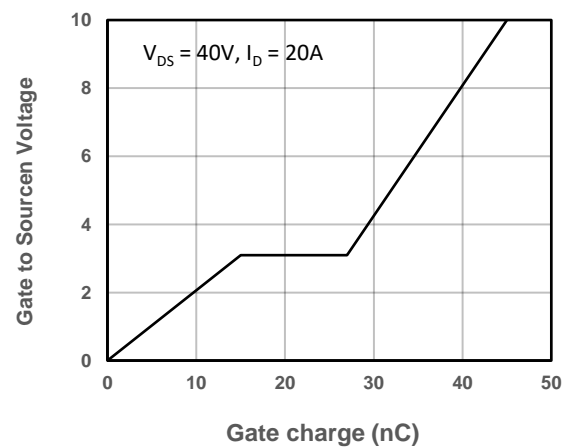
On-Resistance vs. Drain Current and Gate Voltage



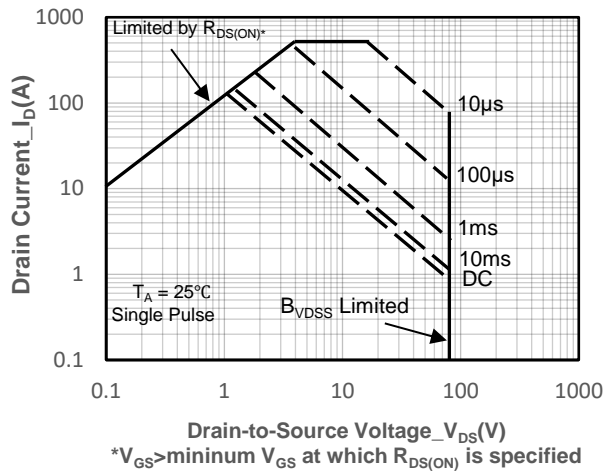
On-Resistance vs. Gate-to-Source Voltage



On-Resistance vs. Junction Temperature

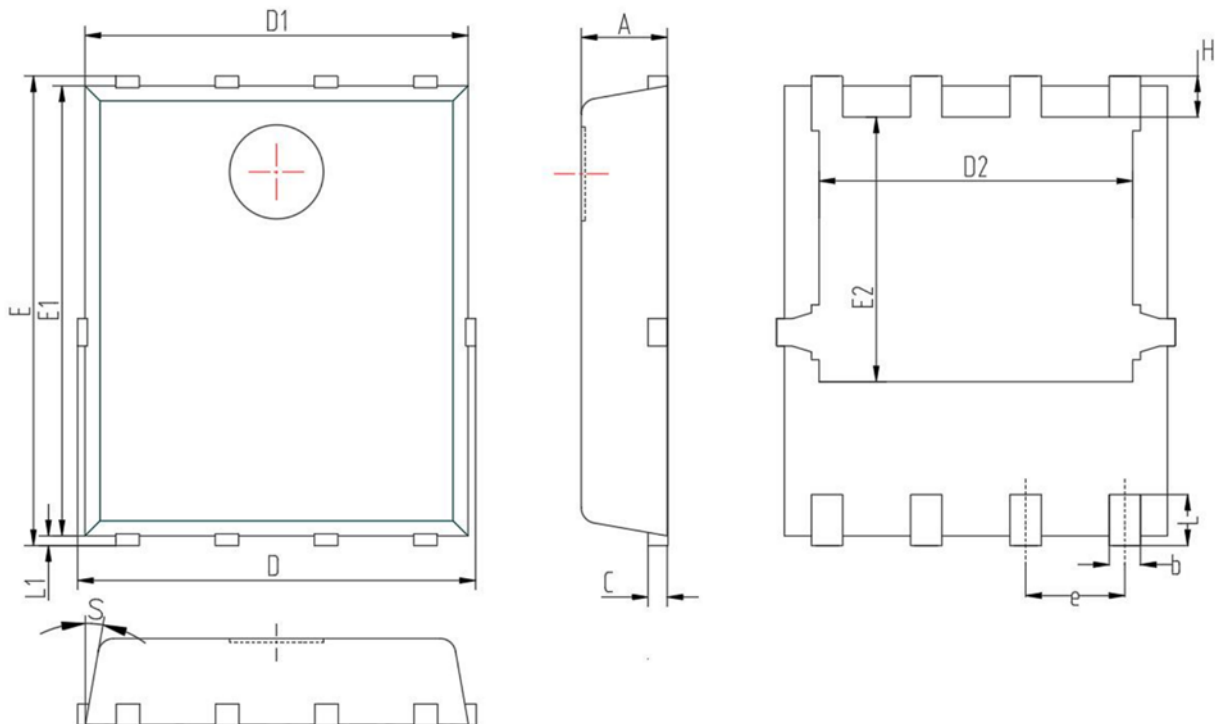


Gate-Source Voltage vs. Gate charge



Safe Operating Area vs. Junction-to-Ambient

➤ Package Information



Symbol	MILL IMETER		
	Min	Nom	Max
A	0.90	1.05	1.20
b	0.25	0.30	0.51
c	0.15	0.25	0.35
D	4.80	5.10	5.40
D1	4.80	5.00	5.20
D2	3.70	4.00	4.30
E	5.80	6.15	6.50
E1	5.50	5.75	5.95
E2	3.30	3.45	3.67
e	1.27BSC		
H	0.40	0.60	0.93
L	0.45	0.65	0.85
L1	0.00	0.10	0.25
S	0°	--	12°



DISCLAIMER

SSCSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. SSCSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENCE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

THE GRAPHS PROVIDED IN THIS DOCUMENT ARE STATISTICAL SUMMARIES BASED ON A LIMITED NUMBER OF SAMPLES AND ARE PROVIDED FOR INFORMATIONAL PURPOSE ONLY. THE PERFORMANCE CHARACTERISTICS LISTED IN THEM ARE NOT TESTED OR GUARANTEED. IN SOME GRAPHS, THE DATA PRESENTED MAY BE OUTSIDE THE SPECIFIED OPERATING RANGE (E.G. OUTSIDE SPECIFIED POWER SUPPLY RANGE) AND THEREFORE OUTSIDE THE WARRANTED RANGE.

OUR PRODUCT SPECIFICATIONS ARE ONLY VALID IF OBTAINED THROUGH THE COMPANY'S OFFICIAL WEBSITE, CRM SYSTEM, OR OUR SALES PERSONNEL CHANNELS. IF CHANGES OR SPECIAL VERSIONS ARE INVOLVED, THEY MUST BE STAMPED WITH A QUALITY SEAL AND MARKED WITH A SPECIAL VERSION NUMBER TO BE VALID.